CLAIMS

What Is Claimed Is:

1. A memory, comprising:

a memory column including,

a plurality of word lines,

a pair of data lines, wherein the plurality of word lines intersects the pair of data lines at intersections, and

memory cells, wherein each memory cell is configured to be accessed by word lines and data lines of an intersection, wherein two distinct word lines of the plurality of word lines may both be active at a same time.

2. The memory of Claim 1, wherein the plurality of word lines includes a first pair of word lines and a second pair of word lines, wherein the first pair of word lines intersect the pair of data lines at a first intersection, wherein the second pair of word lines intersect the pair of data lines at a second intersection, wherein the memory cells include a first memory cell at the first intersection and a second memory cell at the second intersection.

3. The memory of Claim 2, wherein the first pair of word lines includes a first write word line and a first read

word line, wherein the second pair of word lines includes a second write word line and a second read word line.

4. The memory of Claim 3, wherein the two distinct word lines include the first write word line and the second read word line.

5. The memory of Claim 3, wherein the two distinct word lines include the first write word line and the first read word line.

6. The memory of Claim 1, further comprising a latch connected to a write word line, wherein the latch is configured to hold a decoded write word line activation signal of the write word line while a subsequent read word line activation signal of a read word line is being decoded.

7. The memory of Claim 1, wherein the pair of data lines includes a read data line and a write data line, wherein the memory further comprises:

a latch having a latch input and a latch output, wherein the latch input is connected to the read data line and to an input data line, wherein the latch is configured to hold data of the input data line or data of a connected memory cell, wherein the latch output is connected to the write data line.

8. The memory of Claim 7, wherein the memory column further comprises a sense amplifier configured to connect the read data line to the latch, wherein the read data line is connected to a sense amplifier input, wherein a sense amplifier output is connected to the latch input.

9. The memory of Claim 8, wherein when a same memory cell receives a consecutive read access, the memory is configured to read data held in a connected latch of the same memory cell and not data stored in the same memory cell.

10. The memory of Claim 1, wherein at least one of the memory cells is one of:

a three-transistor dynamic memory cell; or

a three-transistor dynamic memory cell including a write transistor, wherein the write transistor is a thin-channel polysilicon transistor having a channel region thickness of 5 nanometers or less.

11. The memory of Claim 8, wherein when a same memory cell receives a consecutive write access from an external input data bus and if the consecutive write access includes new data for a connected latch of the same memory cell, the connected latch and not the same memory

cell is configured to receive the consecutive write access.

12. The memory of Claim 8, further comprising:

a plurality of other memory columns, wherein the other memory columns are configured like the memory column;

a plurality of other sense amplifiers, wherein the other sense amplifiers are configured like the sense amplifier; and

a plurality of other latches, wherein the other latches are configured like the latch.

13. The memory of Claim 12, wherein when a same row of memory cells receives a consecutive read access, the memory is configured to read data held in latches and not data stored in the same row of memory cells.

14. The memory of Claim 12, wherein when a same row of memory cells receives a consecutive write access from an external input data bus and if the consecutive write access includes new data for a particular latch of the same row of memory cells, the particular latch and not a connected memory cell of the particular latch is configured to receive the consecutive write access.

15. The memory of Claim 8, further comprising another memory column configured like the memory column, wherein the memory column and the other memory column share the latch, wherein the memory is configured to conserve space on a silicon die in which the memory is fabricated due to sharing of the latch.

16. A memory, comprising:

a memory column including a pair of data lines having a read data line and a write data line; and

a latch including a latch input and a latch output, wherein the latch input is connected to the read data line and to an input data line, wherein the latch is configured to hold data of the input data line, wherein the latch output is connected to the write data line.

17. The memory of Claim 16, further comprising a sense amplifier configured to connect the read data line to the latch, wherein the read data line is connected to a sense amplifier input, wherein a sense amplifier output is connected to the latch input.

18. The memory of Claim 17, wherein the memory column further includes:

a plurality of word lines, wherein the plurality of word lines intersects the pair of data lines at intersections;

memory cells, wherein each memory cell is configured to be accessed by word lines and data lines of an intersection, wherein two distinct word lines of the plurality of word lines may both be active at a same time.

19. The memory of Claim 18, wherein when a same memory cell receives a consecutive read access, the memory is configured to read data held in a connected latch of the same memory cell and not data stored in the same memory cell.

20. The memory of Claim 17, wherein when a same memory cell receives a consecutive write access from an external input data bus and if the consecutive write access includes new data for a connected latch of the same memory cell, the connected latch and not the same memory cell is configured to receive the consecutive write access.